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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,762	12/26/2001	Mark A. Schmisseur	42390P12808	5769

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/032,762	SCHMISSEUR ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-9,13-15,20-22,27-29,34 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1 and 6* is/are allowed.

6)☒ Claim(s) *9,13-15,20-22,27-29,34 and 35* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is responsive to the arguments filed on 1/3/07.

2. Claims 1, 9, 15, 22, 29 have been amended, claims 2-5, 10-12, 16-19, 23-26, 30-33 have been canceled and no new claims have been added. Thus, claims 1, 6-9, 13-15, 20-22, 27-29, 34-35 are pending.

Claim Objections

Claim 7 is objected to because of the following informalities:

"claim1" in line 1 of claim 7 should be changed to "claim 1".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 9, 13-14, 22, 27-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites "a boot address" in line 7. It is not clear whether it is same or different from "a boot address" recited in line 5. It is necessary to establish a relationship between the two recitations. For the rest of the action it is assumed that same relationship was intended.

Claims 13-14 depend on claim 9. Thus, they carry the same ambiguity of claim 9.

Claim 22 recites "a boot address" in line 8. It is not clear whether it is same or different from "a boot address" recited in line 6. It is necessary to establish a relationship between the two recitations. For the rest of the action it is assumed that same relationship was intended.

Claims 27-28 depend on claim 22. Thus, they carry the same ambiguity of claim 22.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15, 20, 29, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. 5,898,869), in view of Futral et al (US Patent 5925099).

Regarding claim 15, Anderson discloses a method comprising:

- **having a host processing system** (11) **maintain a core processing unit** (13 comprises core processor 31) **in a reset state** (lines 1-5 of column 6 mentioned that the processor 31 is entered and maintained in reset state by asserting HRESET through a hardware/software reset. In addition, lines 9-11 of column 3 mention that the releasing of the suspended processor from reset includes host accessing an address. Thus, the core processing system is maintained in a reset state during power up until released by the host) **during power up of the core processing circuit** (lines 4-6 of column 3 mention that the resetting comprises asserting power-on reset signal. In addition, lines 39-43 of column 7 mention that the reset is asserted during power up of the PCMCIA card. Thus, host maintains the core processing circuit in a reset state during power up of the core processing circuit)
- **transmitting instructions from a system memory of the host processing system** (lines 66-67 of column 2 mention that the PCMCIA downloads code from host) **through a host bridge of the host processing system** (17 is connected to host. Thus, host a bridge to connect 17, which is mentioned as a socket in lines 1-3 of column 8) **and loading the instructions to one or more registers at a boot address associated with the core processing circuit** (column 6, lines 5-15 in view of column 8, lines 7-9, Anderson discloses the "initial program" comprising boot code sequences loaded in the core processing circuit, which must necessarily be loaded to registers. In addition, 115 of Fig 5 shows that the host loads the program to the memory of core. Thus, Anderson discloses loading

instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit), **wherein the instructions are loaded to the boot address** (lines 10-15 of column 6) **in registers formed in a memory** (39) **coupled to the core processing circuit** (31) **through a data bus** (26), **the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state** (lines 5-12 of column 6 mention that the START* by host causes the latch output 61 high, which in turn causes the processor to leave the reset state. These operations are shown in step 117 and 119 in Fig 5. After setting the flip-flop, processor begins booting or initialization as shown in step 121 of Fig 5. Thus, the instructions initialize the core processing circuit upon release of the core processing circuit from the reset state)

- **releasing the core processing circuit from the reset state in response to loading the instructions at the boot address** (column 6, lines 5-12 mention that the processor leaves reset state after the memory is loaded with boot code. In addition, lines 38-39 of column 2 mention that boot logic is configured to release the suspended processor. Thus, the releasing of processor from the reset state is in response to loading the instructions at the boot address);
- **setting an address translation unit** ("address decode circuitry" mentioned in line 48 of column 2 is set by host for causing the processor to boot. The booting occurs from the downloaded code within dual port memory as mentioned in lines

5-15 of column 6) **to enable at least one outbound transaction to fetch instructions from the system memory in response to requests from the core processing unit** (the host sets the address decode circuitry with a particular address for releasing suspended processor execution and causing the processor to boot (lines 30-33 of column 9). The boot program may include diagnostic routine, which can cause further diagnostic routine to be loaded from host as mentioned in lines 28-35 of column 8. Thus, host sets address decode circuitry or address translation unit to activate booting, which again causes to fetch instructions from the host system memory in response to request from the core processing circuit)

- **in response to an outbound transaction, forwarding the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus to the system memory** (since additional routine is loaded from the host memory in response to the query from boot program, an outbound transaction is forwarded from internal bus coupled to core processing circuit to external bus coupled to host system memory).

Although Anderson fetches additional code from memory, Anderson does not explicitly disclose an address translation unit addressed to the system memory, however said transactions would necessarily have to be present in order for the host processing system to properly communicate with the core processing circuit.

Futral et al teach a system where ATU (218) is configured to convert an internal data bus address (204) associated with the outbound transaction to an external data bus address (208) and configured to forward the outbound transaction from an internal data bus (lines 47-67 of column 4) coupled to the core processing circuit (202) to an external data bus coupled to the system memory (201).

It would have been obvious for one ordinary skill in the art to incorporate the ATU within Anderson as proper communication between PCMCIA and host requires translating core bus transaction to host bus transaction.

Regarding claim 29, Anderson discloses an article comprising:

- **a storage medium comprising machine-readable instructions encoded there on for** (there must be a storage media to store the instructions necessary to execute the disclosed methods of Anderson):

- **having a host processing system** (11) **maintain a core processing unit** (13) **in a reset state** (lines 1-5 of column 6 mentioned that the processor 31 is entered and maintained in reset state by asserting HRESET through a hardware/software reset. In addition, lines 9-11 of column 3 mention that the releasing of the suspended processor from reset includes host accessing an address. Thus, the core processing system is maintained in a reset state during power up until released by the host) **during power up of the core processing**

circuit (lines 4-6 of column 3 mention that the resetting comprises asserting power-on reset signal. In addition, lines 39-43 of column 7 mention that the reset is asserted during power up of the PCMCIA card. Thus, host maintains the core processing circuit in a reset state during power up of the core processing circuit)

- **transmitting instructions from a system memory of the host processing system** (lines 66-67 of column 2 mention that the PCMCIA downloads code from host) **through a host bridge of the host processing system** (17 is connected to host. Thus, host a bridge to connect 17, which is mentioned as a socket in lines 1-3 of column 8) **and loading the instructions to one or more registers at a boot address associated with the core processing circuit** (column 6, lines 5-15 in view of column 8, lines 7-9, Anderson discloses the "initial program" comprising boot code sequences loaded in the core processing circuit, which must necessarily be loaded to registers. In addition, 115 of Fig 5 shows that the host loads the program to the memory of core. Thus, Anderson discloses loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit), **wherein the instructions are loaded to the boot address** (lines 10-15 of column 6) **in registers formed in a memory** (39) **coupled to the core processing circuit** (31) **through a data bus** (26), **the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state** (lines 5-12 of column 6 mention

that the START* by host causes the latch output 61 high, which in turn causes the processor to leave the reset state. These operations are shown in step 117 and 119 in Fig 5. After setting the flip-flop, processor begins booting or initialization as shown in step 121 of Fig 5. Thus, the instructions initialize the core processing circuit upon release of the core processing circuit from the reset state)

- **releasing the core processing circuit from the reset state in response to loading the instructions at the boot address** (column 6, lines 5-12 mention that the processor leaves reset state after the memory is loaded with boot code. In addition, lines 38-39 of column 2 mention that boot logic is configured to release the suspended processor. Thus, the releasing of processor from the reset state is in response to loading the instructions at the boot address);
- **setting an address translation unit** ("address decode circuitry" mentioned in line 48 of column 2 is set by host for causing the processor to boot. The booting occurs from the downloaded code within dual port memory as mentioned in lines 5-15 of column 6) **to enable at least one outbound address to address location in system memory to fetch instructions from the system memory in response to requests from the core processing unit** (the host sets the address decode circuitry with a particular address for releasing suspended processor execution and causing the processor to boot (lines 30-33 of column 9). The boot program may include diagnostic routine, which can cause further diagnostic routine to be loaded from host as mentioned in lines 28-35 of column

8. Thus, host sets address decode circuitry or address translation unit to activate booting, which again causes to fetch instructions from the host system memory in response to request from the core processing circuit)

Although Anderson fetches additional code from memory, Anderson does not explicitly disclose an address translation unit addressed to the system memory, however said transactions would necessarily have to be present in order for the host processing system to properly communicate with the core processing circuit.

Futral et al teach a system where ATU (218) is configured to convert an internal data bus address (204) associated with the outbound transaction to an external data bus address (208) and configured to forward the outbound transaction from an internal data bus (lines 47-67 of column 4) coupled to the core processing circuit (202) to an external data bus coupled to the system memory (201).

It would have been obvious for one ordinary skill in the art to incorporate the ATU within Anderson as proper communication between PCMCIA and host requires translating core bus transaction to host bus transaction.

Regarding claims 20 and 34, Anderson discloses all of the limitations of respective independent claims 15 and 29, as noted above. However, though Anderson discloses the additional instructions comprising "diagnostic routines" (column 3, lines 13-14),

Anderson does not explicitly disclose the system wherein the additional instructions comprise instructions to commence a power-on self test procedure. The examiner takes Official Notice that power-on self test procedures are a well known type of diagnostic routine. It would have been obvious at the time that the invention was made to use power-on self test procedures for the diagnostic routines disclosed by Anderson.

The motivation for doing so would have been to assure the integrity of the information stored on the core processing circuit.

4. Claims 21 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. 5,898,869), in view of Futral et al (US Patent 5925099), further in view of Klein (U.S. 6,216,224).

Regarding claims 21 and 35, Anderson or Futral does not disclose the method wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

Klein teaches the method wherein the (additional) instructions further comprise instructions to launch an operating system to the core processing circuit (column 4, lines 13-15) in order to "bring the PC up to a state that can be used by a human operator" (page 2, column 4, lines 16-17). It would have been obvious to one of ordinary skill in the ad at the time of invention to incorporate Klein's teachings of loading the

operating system with Anderson's disclosure of a system comprising a core processing circuit initialization with a host processing system. The motivation for doing so would have been to accommodate for the use of the system by a human operator.

Allowable Subject Matter

Claims 1, 6 are allowed.

Claims 7-9, 13, 14, 22, 27-28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Response to Arguments

Applicant's arguments filed on 1/3/07 with respect to claims 15 and 29 have been fully considered but they are not persuasive.

Applicant argues that host processor of Anderson does not maintain the core processing circuit in a reset state during power up of the core processing circuit, since flipflop 55 performs this function instead of host.

Examiner disagrees. Applicant admitted that host initiates reset. The reset is maintained by Q output of 61. The Q output is made lower by host so that 31 can enter into reset state. 31 is maintained is reset state by the lowering of Q output. Next access by host to PCMCIA causes assertion of START* signal. This signal causes 61 to go high so that

processor can be released (lines 1-15 of column 6). Therefore, Q output is controlled by host and the processor 31 is maintained in reset state by host.

Applicant further argues that there is no host bridge on the host as 17 is on PCMCIA card.

Examiner disagrees. There is a socket on host side for connecting PCMCIA card (lines 1-5 of column 8), which is the host bridge.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116